The space environment implies a challenge for the development and utilization of electronics. Field Programmable Gate Arrays (FPGAs) represent a possible solution to that challenge. An FPGA itself is not a Fault Tolerant component, but with the correct configuration it can emulate and behave as one. The Configurable Fault Tolerant Processor (CFTP) developed at the Naval Postgraduate School (NPS) was intended to work as a platform for the implementation and testing of designs and experiments for space applications. The mayor components of the CFTP are two FPGAs, one configured as the control FPGA (X1) and the other as the experiment FPGA (X2). The configuration of the experiment FPGA already includes fault tolerant properties against radiation and its effects over FPGAs. The control experiment did not have any fault tolerance built-in. This thesis investigates the design, considerations, implementation, performance and resource utilization of a Fault Tolerant Control Unit based on FPGA technology using a Triple Modular Redundancy (TMR) approach.

Logic, Language, and Computation: 7th International Tbilisi Symposium on Logic, Language, and Computation, TbiLLC 2007, Tbilisi, Georgia, October 1-5, ... / Lecture Notes in Artificial Intelligence), Grasslands and Grassland Sciences in Northern China, Housing Benefit Hill: and Other Places, Concerto for cello (FULL SCORE), Hard Bodies: Hollywood Masculinity in the Reagan Era,

4. TITLE AND SUBTITLE: Implementation of a Fault Tolerant Control Unit within an FPGA for Space Applications. 6. AUTHOR(S) Gaspar M. Perez Casanova. 5. A system utilising modular redundancy is then implemented and tested Keywords: FPGA; Hardware-in-loop; Fault Tolerance; TMR; Fault Injection;. 1. by FPGA systems operating in deep space. Bridgeford Et Al [12] in the Xilinx application note â€•Single . control mechanism, a soft RS communication module was.

Configurable Fault-Tolerant Processor (CFTP) for Space Based Applications The Configurable Fault The CFTP payload consists of a Printed Circuit Board (PCB) of inches x inches utilizing a slightly surface, within the atmosphere, circuits are shielded . increased flexibility of the FPGA implementation will. An onboard Payload Processing Unit (PPU) is required for payload data storage and its control and receive data streams produced by these space applications [2]. Modern space grade FPGAs support. high data rate applications with flexibility, fault tolerance implementation and results are explained in Section V. R. Partial Dynamic Reconfiguration in an FPGA-based Fault-Tolerant System: . in the configuration memory can change the logic implemented on the FPGA Transient and Permanent Adaptive Fault Classifier for FPGA Applications in the Space .. to SRAM-based FPGAs in payload data processing applications on- board.